Remarks

This is a reply to the outstanding non-final Office Action, dated June 21, 2002, in which concurrently filed herewith is a Petition for Extension of Time covering the three-month extended time period for filing this response including the required fee amount thereto. (An authorized Credit Card Payment Form, covering the fee amount for the extended period of time, is enclosed herewith.)

A minor informality discovered in the Substitute Specification is being corrected herein.

By the amendments presented hereinabove, previously pending claims 1, 3, 22, 24, 26, 27, 29, 32 and 36 were amended, claims 25 and 28 were canceled and claims 37 – 38 were newly presented. Amendments were made to these claims in consideration of further clarifying the subject matter intended to be covered including in terms of more clearly defining the same over the art documents, as cited in the standing rejections. For example, base claim 1 now calls for a semiconductor integrated circuit device scheme including at least two zener diodes connected in series and having for a structural configuration such as that shown in the example illustrations in Figs. 3-5 of the drawings, although not limited thereto. Independent claims 29 and 36 were amended to define a scheme calling for a first diode and a second diode connected in series and similarly covering a structural configuration such as that shown in Figs. 3-5 of the drawings, etc., although not limited thereto. Independent claim 32 was amended to further clarify the structural device scheme such as for a single diode, for example, a zener diode, configured as that shown in Figs. 3-5, as well as at the right most portion of Figs. 20 and 24, regarding the zener diode thereof, although not limited thereto.

Regarding canceled claim 25, moreover, the further limiting aspects included in the first portion thereof were incorporated into that of base claim 1 and the second portion of canceled claim 25 is included in dependent claim 24, as now amended. Regarding canceled claim 28, the first and third parts thereof were incorporated into that of base claim 1, the second part thereof is contained in dependent claim 27, as now amended, and the last part thereof relating to the wiring is now contained in amended claim 1.

The semiconductor IC device scheme according to claim 1 calls for at least two zener diodes that are connected in series, each of which includes a well region of a first conductivity type formed on a semiconductor substrate of a second conductivity type (e.g., p well 5 formed in n-type substrate/well 3); a first semiconductor region of the second conductivity type formed in the well region (e.g., n^+ region 20); and a second semiconductor region of the first conductivity type formed in the well region at the bottom portion of (i.e., beneath) the first semiconductor region and being smaller in area, defined by a planar pattern, than that of the first semiconductor region (e.g., p^+ region 6 which is formed in the same well region 5, beneath region 20, and covers a smaller area than region 20 in Figs. 3-4, etc.). The device according to base claim 1 also now calls for a plurality of first connection holes for electrically connecting therethrough each of the first semiconductor regions and, also, calls for a plurality of second connection holes for electrically connecting therethrough each of the well regions. This can be seen from the example illustration in Figs. 3 and 4 of the drawings in which connection holes 24 are provided for effecting electrical connection therethrough to the respective n^+ regions 20 and connection holes 25 are for effecting electrical connection to the p well 5.

According to base claim 1, as now amended, also, a wiring is formed over the insulating film and electrically connecting the first connection holes (e.g., 24 as it relates to zener diode D2) and the second connection holes (e.g., 25 as it relates to the zener diode D1 section of Fig. 4 of the drawings). As can be seen from Fig. 4 of the drawings, the cathode side of the diode D2 (i.e., region 20) is connected via connection hole 24, wire 22, connection hole 25 and heavily doped contact region 19 to the p well region associated with diode D1. The invention according to claim 1 also features a scheme in which the plurality of first connection holes (e.g., 24) are located "outside a junction formed between said first semiconductor region and said second semiconductor region", similarly as that shown in the various example embodiments of the present application including with regard to Fig. 4 of the drawings in which, it is noted, the through holes 24 are located at that part of the "first semiconductor region" outside the area covered by region 6 (which forms a PN junction with region 20). The additional featured aspects included in the "wherein" clause of base claim 1 relate to the effected diode resulting from the first PN junction formed between the semiconductor region 20 and that of region 6 in Fig. 4, as one example, and, further, the second PN junction that is formed between the semiconductor substrate (e.g., well region/substrate 3) and well region 5, the latter necessarily having a breakdown voltage greater than that of the first PN junction formed by regions 6 and 20.

Claim 2 (dependent on base claim 1) further characterizes the invention by calling for the "second semiconductor region" to be arranged centrally to that of the first semiconductor region and, moreover, for the "plurality of first connection holes" to be "arranged at a periphery of said first connection

semiconductor region". These featured aspects are similar to that shown by the relationship of the region 6 and that of region 20 with regard to Figs. 3 and 4 of the drawings, etc. Dependent claim 3 further characterizes the device as one in which a junction depth of the first semiconductor region in a region in which the first and second semiconductor regions form a junction is shallower than that part thereof which forms a junction with the well region. This can be seen from Fig. 4 of the drawings, although not limited thereto, in which the outer peripheral portion of the region 20 is extended deeper into the well than is the junction between region 20 and region 6. Paragraphs [0045] and [0046] give a detailed discussion of the device structure such as it relates to Figs. 3 and 4 of the drawings and as discussed hereinabove. The conductivity type relationships of the particular regions/well regions as well as the size/placement relationships between that of p^+ region 6 and that of n^+ region 20 is given in paragraph [0045] and the depth relationship of the junction as it relates to different parts of the n^+ region 20 is given in paragraph [0046]. The wire connections of the invention such as shown in Figs. 3 and 4 of the drawings, are discussed in paragraphs [0047]/[0048], etc.. Such featured aspects are contained -- although in a somewhat different fashion-- in each of independent claims 1, 29, 32 and 36. Further defining aspects directed thereto are detailed with regard to the corresponding dependent claims. It is submitted, such a scheme as that now called for in claims 1+, 29+, 32+ and 36 is a clear and patentable improvement over that previously known including over the art documents as cited in the outstanding rejections.

According to the outstanding Office Action, claims 1-3, 22, 24,26, 27 and 29-35 were rejected under 35 USC §102(b) as anticipated by Vinn et al (US

4,646,114); and claims 1-3, 22 and 24-36 were rejected under 35 USC §103(a) over the combination of Howard Jr., (US 3,881,179) in view of Matthews (US 5,691,554). It will be shown, hereinbelow, the invention according to claims 1+, 29+, 32+ and 36 was neither anticipated nor could it have been achievable in a manner as that alleged in the standing rejections. Therefore, insofar as presently applicable, including with regard to the newly added claims, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

According to the present invention, the connection holes such as connection holes 24 in Fig. 3, for connecting the wires 21 and 22 and the n^+ region 20 to each other are not arranged at a location, with respect to a plan view thereof, of the junction formed between that of n^+ region 20 and p^+ region 6. That is, those connection holes 24 are not arranged at a center portion of the region 20. Rather, such connection holes are arranged outside the center portion of the n^+ region 20, namely, at an outer periphery portion thereof at which the junction depth is deeper than the more central portion thereof. As explained in the Specification, in comparison with a case in which the connection holes 24 are arranged at the upper part of the p^+ region 6, the junction depth of the n^+ region 20 at the bottom of the respective hole 24 becomes great, and the generation of a tunnel current in this region becomes restricted. Thus, the propensity for leakage current at voltages less than the breakdown voltage of the device is substantially reduced (Paragraphs [0052]-[0053] on pages 16-17 of the Substitute Specification). Additionally, providing the connection holes to the diode at a location outside the plan view area covered by the PN junction forming the zener diode also leads to a further reduction in leakage current

(Paragraph [0087] on page 32 of the Substitute Specification). The invention according to claims 1+, 29+, 32+ and 36 calls for such a scheme which overcomes problems of leakage currents as well as others, which are discussed in greater detail in the Specification.

According to base claim 1, the invention therein further calls for the "second PN junction" that is formed between the semiconductor substrate (e.g., 3 in Fig. 4) and the well region (e.g., 5) to have " a breakdown voltage greater than that of said first PN junction" (defined by a junction between the "first semiconductor region" (e.g., n^+ 20) and the "second semiconductor region" (e.g., p^+ region 6 in Fig. 4). A similar such featured aspect is called for, also, with regard to independent claims 32 and 36, although those claims may be somewhat differently presented than claim 1.

When designing a zener diode such as a structural scheme shown in Fig. 4 of the drawings, although not limited thereto, it is necessary for such a scheme to be designed with doping concentrations such that the breakdown voltage effected between the n region 3 and p well 5 to have a greater breakdown voltage than that across the junction between p^+ region 6 and n^+ region 20. Such is achieved in connection with the present invention. Also, with regard to a multi-stage series connection of zener diodes, for example, the breakdown voltage requirements of a structure as that shown in Fig. 4 may be that shown in attached **Sketch 1**, which is consistent with that defined in the claims. With regard to Sketch 1, for example, which relates to the series connection of two zener diodes as shown in Figs. 2 and 4 of the drawings, D1 and D2 relate to the zener PN junction formed between that of the p^+ region 6 and n^+ region 20 of the D1 portion of Fig. 1, while D1' relates to a junction effected between p region 3

and p well 5 in the D1 portion, and D2' relates to the junction formed between the p region 3 and the p well 5 with regard to portion D2. The breakdown voltage of D1' must be equal to or greater than that of the breakdown voltage of the corresponding zener diode junction D1. Moreover, the breakdown voltage of D2' should be equal to the overall breakdown voltage of D1 + D2. Consistent with this, it is noted that the p type wells 5 according to the example embodiments of the present application have a lighter doping concentration than that of the p^+ region 6 which leads to a series connection of zener diodes that operates satisfactorily. It is submitted, such a scheme as that now called for in each of the independent claims and, also, with regard to the corresponding dependent claims thereof, could not have been anticipated nor rendered obvious in a manner as that alleged in the rejections.

Vinn et al schemed a zener diode structure having an n-type epitaxial layer 14, a p-type buried layer 40 and an n-type region 20 including protrusions 30 and 32. A zener junction is formed between p-type buried layer 40 and n-type region 20. A cathode electrode 46 is formed on the n-type region 20. (Column 4, lines 8-52, and Fig. 2 in Vinn et al.) In other words, a through hole for the electrode 46 is formed on the zener junction, which is in clear contradistinction with that presently called for. As can be seen from each of the independent claims 1+, 29+, 32 and 36, of the present invention, the first connection holes (e.g., 24 in Figs. 3 and 4 of the present application) are formed over a plan view area outside an area covered by the PN junction of the effective zener diode. For these and other reasons, the invention according to claims 1+, 29+ and 32+ could not have been anticipated by Vinn et al.

Howard et al disclosed a scheme for a zener diode structure having an

n-type cathode 32, a p-type conductive portion 21 and a p^+ -type anode 22 connected with the p-type conductive portion 21. As can be seen from the Fig. 1 illustration thereof, for example, the p^+ -type anode 22 is laterally surrounded by an n-type epitaxial region 16 and by an n^+ -type buried layer 12, therebelow. A zener junction is formed between the n-type cathode 32 and the p^+ -type anode 22. A terminal C is located at a point remote from the shallowest portions of the n-type cathode 32, to avoid "spike-through" or shorting problems which might otherwise be caused by the aluminum extending through junction 36. (Column 4, line 67, to column 5, line 46, and Fig. 1 in Howard et al.)

If one of ordinary skill were to attempt to apply Howard et al's zener diode to a multi-step scheme including two or more series connected zener diodes, it would be quite difficult for the zener diode to keep the stability in the breakdown voltage between the n^+ -type buried layer 12 and the p^+ -type anode 22 due to the presence of the high concentration associated with the p^+ -type anode 22. That is, if Howard et al desired to design a device including a multi-stage zener diode series connection arrangement, the p^+ -type anode 22, it is submitted, must necessarily have a lower concentration than that of the n^+ -type buried layer 12, in Fig. 1, which would be contrary to Howard et al's structure. In other words, one of ordinary skill would not have been led to achieve the key points of applicants invention such as called for in each of the independent claims, as now amended. Moreover, there is no teaching or suggestion of why one of ordinary skill would have attempted to achieve a scheme as that presently called for, from Howard et al's teachings.

Matthews et al disclosed a zener diode 20 (e.g., Fig. 3) having a p^+ -type region 39 which forms the cathode connection for the zener diode 20 and an

n^+ -type region 38 (N anode) on the surface of p-type substrate 34. A p^- -type region (p field implant) 40 is formed nearby the p^+ type region 39. Since the p^- -type region (p field implant) 40 is formed away from the n^+ -type region (anode 38), the breakdown voltage at the corner of the n^+ -type region 38 is raised. (Column 3, lines 34-64, and Fig. 3, in Matthews et al.) Accordingly, Matthews et al's teachings do not overcome the deficiency discussed above with regard to Howard et al's disclosure. That is, Matthews et al failed to overcome the deficiencies in Howard et al's disclosure, and for the same and similar reasons therefor, a multiple-stage series connection of zener diodes could not have been practically schemed. Moreover, Howard, it is submitted, did not appear to address problems of leakage current, etc., which have led the present inventors to achieve the present invention, as that presently called for in claims 1+, 29+, 32+ and 36. That is, there is no reason or motivation that would have led Howard Jr., to redesign his zener diode scheme differently, from Matthews teachings, which would have led to applicants invention. Any such redesign could have been realized, it is submitted, only through prior knowledge of applicants disclosure. For these and other reasons, therefore, the invention according to claims 1+, 29+, 32+ and 36 could not have been achievable even in view of the combined teachings of Howard Jr., and Matthews.

Newly added claim 37 (dependent on claim 29) similarly calls for the breakdown voltage relationship such as that called for in independent claims 1+, 32+ and 36. Newly added claim 38 (also dependent on claim 29) similarly features a doping concentration relationship between that of the third semiconductor region (e.g., p^+ region 6) and the "first semiconductor region" (e.g., p well 5), similarly as that found in dependent claim 24, for example. For

the same and similar reasons as that argued above, applicants submit, these claims are also considered allowable.

Therefore, in view of the amendments presented hereinabove, together with these accompanying remarks, reconsideration and withdrawal of the previously standing rejections as well as a favorable action therefor on all of the presently pending claims, i.e., claims 1-3, 22 and 24-36, directed to the previously elected invention, and an early formal Notification of Allowability of the above-identified application is respectfully requested.

A marked-up version showing changes made is enclosed herewith.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (843.39542X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
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703-312-6600
Enclosures: Sketch 1

MARKED-UP VERSION SHOWING CHANGES MADE

IN THE SUBSTITUTE SPECIFICATION:

On Page 22, please **replace** paragraph [0067], bridging to page 23, with the following:

[0067] Next, as shown in FIG. 17, each of side wall spacers 18 is formed on respective side walls of gate electrodes 10 and 11. Then, boron (B) ions are implanted into the n type scattering layer 3 and the n type well 4 and thereby a [p^- type] p^+ type semiconductor region (source and drain) 19 with high impurity concentration is, respectively, formed in a memory cell forming region and a peripheral circuit forming region. Although not shown in the figure, a p^+ type semiconductor region 19 is also formed at a part of the p type well 5 in the zener diode forming region (at the lower part of the connection hole 25 shown in FIG. 4) at this time. In addition, arsenic (As) ions and phosphor (P) ions are implanted into the p type well 5, and thereby a n^+ type semiconductor region (source and drain) 20 with high impurity concentration is formed in a peripheral circuit forming region. And, the n^+ type semiconductor region 20 with high impurity concentration is formed in a zener diode forming region. The side wall spacers 18 are formed by performing isotropic etching of a silicon oxide film (not shown) deposited on the substrate 1 by using the CVD method. At this time, dose quantity of boron ion is defined as 2×10^{15} cm^{-2} and implantation energy thereof is defined as 10 keV. Dose quantity of arsenic ion is defined as 3×10^{15} cm^{-2} and

implantation energy thereof is defined as 60 keV. And, dose quantity of phosphor ion is defined as 5×10^{13} cm^{-2} and implantation energy thereof is defined as 60 keV.

IN THE CLAIMS:

Please **amend** claims 1, 3, 22, 24, 26, 27, 29, 32, 36, as follows:

1. **(Thrice Amended)** A semiconductor integrated circuit device comprising:

a semiconductor substrate of a [first] second conductivity type;

[a] at least two or more two zener diodes connected in series each comprised of:

a well region of a first conductivity type formed on said semiconductor substrate;

a first semiconductor region of [a] said second conductivity type formed in [a primary face of said semiconductor substrate] said well region, and

[and] a second semiconductor region of said first conductivity type formed in said well region [said semiconductor substrate] at a bottom portion of said first semiconductor region and being smaller in area, defined by a planar pattern thereof, than said first semiconductor region,

an insulation film formed over a primary face of said semiconductor substrate; and

a plurality of first connection holes for electrically connecting therethrough said first semiconductor region and a plurality of second connection holes for

electrically connecting therethrough said well region, both of which are formed in said insulation film;

wherein a wiring is formed over said insulation film and electrically connecting said first connection holes of a first of said zener diodes and said second connection holes of a second said zener diodes, said plurality of first connection holes, for electrically connecting said first semiconductor region and a wire to each other, are arranged in a region located outside a junction formed between said first semiconductor region and said second semiconductor region of said first zener diode, a first PN junction formed between said first semiconductor region and said second semiconductor region functions as a diode device, and a second PN junction is formed between said semiconductor substrate and said well region and has a breakdown voltage greater than that of said first PN junction .

3. **(Amended)** A semiconductor integrated circuit device according to claim 1, wherein a junction depth of said first semiconductor region in a region in which said first and second semiconductor regions form a junction is shallower than that of said first semiconductor region in a region in which said well region and said first semiconductor region form a junction.

22. **(Twice Amended)** A semiconductor integrated circuit device according to claim 2, wherein a junction depth of said first semiconductor region in a region in which said first and second semiconductor regions form a PN junction is shallower than that of said first semiconductor region in a region in

which said [semiconductor substrate] well region and said first semiconductor region form a PN junction.

26. **(Amended)** A semiconductor integrated circuit device according to claim 1, wherein said second semiconductor region has an impurity concentration higher than that of said [semiconductor substrate] well region.

27. **(Amended)** A semiconductor integrated circuit device according to claim 22, wherein said second semiconductor region has an impurity concentration higher than that of said [semiconductor substrate] well region.

29. **(Amended)** A semiconductor integrated circuit device comprising:

a first diode and a second diode connecting in series, each of said first and second diode including:

a first semiconductor region of a first conductivity type being formed in a semiconductor substrate;

a second semiconductor region of a second conductivity type, the second semiconductor region being formed [on] in said first semiconductor region;

a third semiconductor region of a first conductivity type, the third semiconductor region being formed [over] in said first semiconductor region and under said second semiconductor region; and

an insulation film formed over a primary face of said semiconductor substrate; and

[having] a plurality of first connection holes for electrically connecting therethrough said second semiconductor region and [wiring], a plurality of

second connection holes, formed in said insulation film, for electrically connecting therethrough said first semiconductor region, both of which are formed in said insulation film,

wherein a wiring is formed over said insulation film and electrically connecting said first connection holes associated with said first diode and said second connection holes associated with said second diode, a first PN junction formed between said second semiconductor region and said third semiconductor region functions as a diode device, said third semiconductor region has an impurity concentration higher than that of said first semiconductor region, said second semiconductor region has a first portion and a second portion, the first portion is that in which a PN junction is formed between said third semiconductor region and said second semiconductor region and the second portion is that below which said third semiconductor region is not formed, a junction depth of said first portion is shallower than that of said second portion, said second portion is formed outside said first portion, and said first connection holes are formed over said second portion of said second semiconductor region.

32. **(Amended)** A semiconductor integrated circuit device comprising:

a first well region of a first conductivity type being formed in a semiconductor substrate;

a second well region of a second conductivity type being formed in said first well region;

a first semiconductor region of [a] said first conductivity type, the first semiconductor region being formed [over a semiconductor substrate] in said second well region;

a second semiconductor region of [a] said second conductivity type, the second semiconductor region being formed in said second well region under said first semiconductor region; and

an insulation film formed over a primary face of said semiconductor substrate and having a plurality of first connection holes for electrically connecting therethrough said first semiconductor region and wiring,

wherein said first semiconductor [portion] region has a first portion and a second portion, the first portion is that below which said second semiconductor region is formed and the second portion is that below which said second semiconductor region is not formed, a first PN junction is formed between said second semiconductor region and said first semiconductor region at said first portion and functions as a diode device, said second portion is formed outside said first portion, [and] said first connection holes are formed over said second portion of said first semiconductor region, and second semiconductor region has an impurity concentration higher than that of said second well region, and a second PN junction is formed between said first well region and said second well region and has a breakdown voltage greater than that of said first PN junction.

36. **(Amended)** A semiconductor integrated circuit device comprising a first diode and a second diode connected in series and formed in a first well region, the first well region being formed on a semiconductor substrate, said first diode and said second diode, respectively, comprising:

a second well region of a first conductivity type, the second well region being formed in said first well region which is of a second conductivity type;

[a first conductivity type well region formed on a semiconductor substrate;]

a first semiconductor region of a second conductivity type, the first semiconductor region being formed [on] in said second well region;

a second semiconductor region of a first conductivity type, the second semiconductor region being formed in said second well region and under said first semiconductor region; and

an insulation film formed over a primary face of said semiconductor substrate; and

[having] a plurality of first connection holes for electrically connecting therethrough said first semiconductor region and [wiring] a plurality of second connection holes for electrically connecting therethrough said second well region, both of which are formed in said insulation film,

wherein a wiring formed on said insulation film and connection with said first connection holes in said first diode and said second connection holes in said second diode said second semiconductor region has an impurity concentration higher than that of said second well region, said first semiconductor region has a first portion and a second portion, the first portion is that below which said second semiconductor region is formed and the second portion is that below which said semiconductor region is not formed, a first PN junction is formed between said second semiconductor region and said first semiconductor region at said first portion and constitutes a zener diode, a junction depth of said first portion is shallower than that of said second portion, said second portion is formed in a periphery of said first portion so as to surround said first portion, [and] said plurality of first connection holes are arranged over said second portion so as to surround said first portion, and a second PN junction is formed

between said first well region and said second well region and has a breakdown voltage greater than that of said first PN junction.